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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)			Complete if Known Application Number: 10/755,042 Filing Date: January 9, 2004 First Named Inventor: MOU-SHIUNG LIN Art Unit: 2815 Examiner Name: JEROME JACKSON, JR.		
Sheet	1	of	3	Attorney Docket No: 085027-0104	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1	MISTRY, K. et al. "A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," IEEE International Electron Devices Meeting (2007) pgs. 247-250	
	2	EDELSTEIN, D.C., "Advantages of Copper Interconnects," Proceedings of the 12th International IEEE VLSI Multilevel Interconnection Conference (1995) pgs. 301-307	
	3	THENG, C. et al. "An Automated Tool Deployment for ESD (Electro-Static-Discharge) Correct-by-Construction Strategy in 90 nm Process," IEEE International Conference on Semiconductor Electronics (2004) pgs. 61-67	
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	5	YEOH, A. et al. "Copper Die Bumps (First Level Interconnect) and Low-K Dielectrics in 65nm High Volume Manufacturing," Electronic Components and Technology Conference (2006) pgs. 1611-1615	
	6	HU, C-K. et al. "Copper-Polyimide Wiring Technology for VLSI Circuits," Materials Research Society Symposium Proceedings VLSI V (1990) pgs. 369-373	
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	9	YEOH, T-S. "ESD Effects On Power Supply Clamps," Proceedings of the 6th International Symposium on Physical & Failure Analysis of Integrated Circuits (1997) pgs. 121-124	
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	11	VENKATESAN, S. et al. "A High Performance 1.8V, 0.20 pm CMOS Technology with Copper Metallization," Technical Digest IEEE International Electron Devices Meeting (1997) pgs. 769-772	
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	22	LUTHER, B. et al. "Planar Copper-Polyimide Back End of the Line Interconnections for ULSI Devices," Proceedings of the 10th International IEEE VLSI Multilevel Interconnection Conference (1993) pgs. 15-21	
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